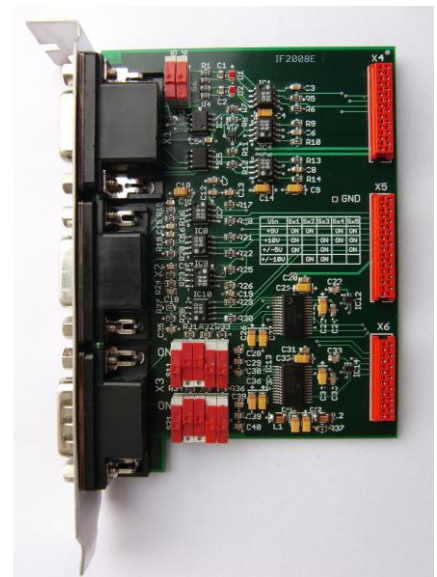
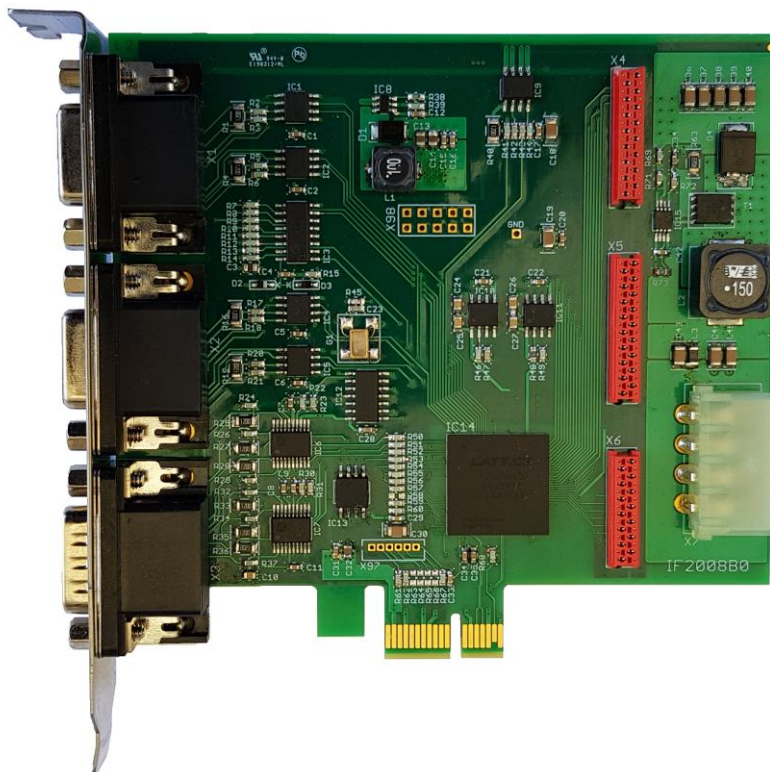


## Description

**IF2008/PCIe** PCI Basis Board  
**IF2008E** Expansion Board



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# 1 Technical Data

## 1.1 IF2008/PCIe Basis Board

### **Mechanics and environment**

- Dimensions (PCB) approx. 110 x 105 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C
- 2x D-SUB female connectors HD 15-pin for sensor connections
- 1x D-SUB male connector HD 15-pin for encoder signals
- 1x Tyco/AMP Commercial MATE-N-LOK connector (IDE hard-drive connector) for supply of DC/DC converter
- 3x Tyco/AMP MicroMatch female connectors for connection to IF2008E

### **PCI-Express bus**

- PCI-Express x1 interface
- Target interface (slave) according to specification Rev 1.0)
- Current consumption at +3.3 V approx. 0.5 A, without sensors and encoders
- Power supply of encoders with +5 V from the PCI power
- Power supply of the sensors with +24 V from the PC power supply

### **Sensor interface (X1 / X2)**

- 4x RS422 drivers (2x TxD and 2x trigger out) and 2x RS422 receivers per connector (input/output frequency max. 5 MHz)
- Power supply of sensors with 24 V

### **Encoder interface (X3)**

- Interface for two encoders with 1Vss, RS422 (difference) or TTL (single-ended) signals
- Power supply of the encoders with +5 V from PCI power supply without galvanic isolation (current consumption dependent on the connected encoders)
- Interpolation programmable from 1 to 64 times for encoders with 1Vss signals (input frequency max. =  $[3.2 \text{ MHz} / \text{interpolation}] \leq 800 \text{ kHz}$ )
- Evaluation programmable from 1 to 4 times for encoders with:
  - Rs422-/Difference signals (input frequency max. 800 kHz)
  - TTL-/Single-ended signals (input frequency max. 400 kHz)

## 1.2 IF2008E Expansion Board

### **Mechanics and environment**

- Dimensions (PCB) approx. 71 x 102 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C
- 1x D-SUB female connector HD 15-pin for sensor connections
- 1x D-SUB female connector 9-pin for IO interface
- 1x D-SUB male connector 9-pin for analog inputs
- 3x MicroMatch female connectors for connection to IF2008/PCIe

### **Sensor interface (X1)**

- Identical to IF2008/PCIe (X1)

### **IO interface (X2)**

- 4x Optocoupler inputs, input current max. 5 mA, input frequency max. 1 MHz
- 4x Optocoupler outputs, output current max. 20 mA, output frequency max. 1 MHz

### **Analog interface (X3)**

- 2x ADC channels
- Input voltage range 0-5 V, 0-10 V,  $\pm 5$  V,  $\pm 10$  V, separately adjustable for each channel via DIP switch
- Resolution 16 bits
- Offset error max.  $\pm 3$  mV
- Gain error max.  $\pm 5$  mV
- Conversion rate max. 150 kHz per channel

## 2 Hardware

### 2.1 View of IF2008/PCle Basis Board

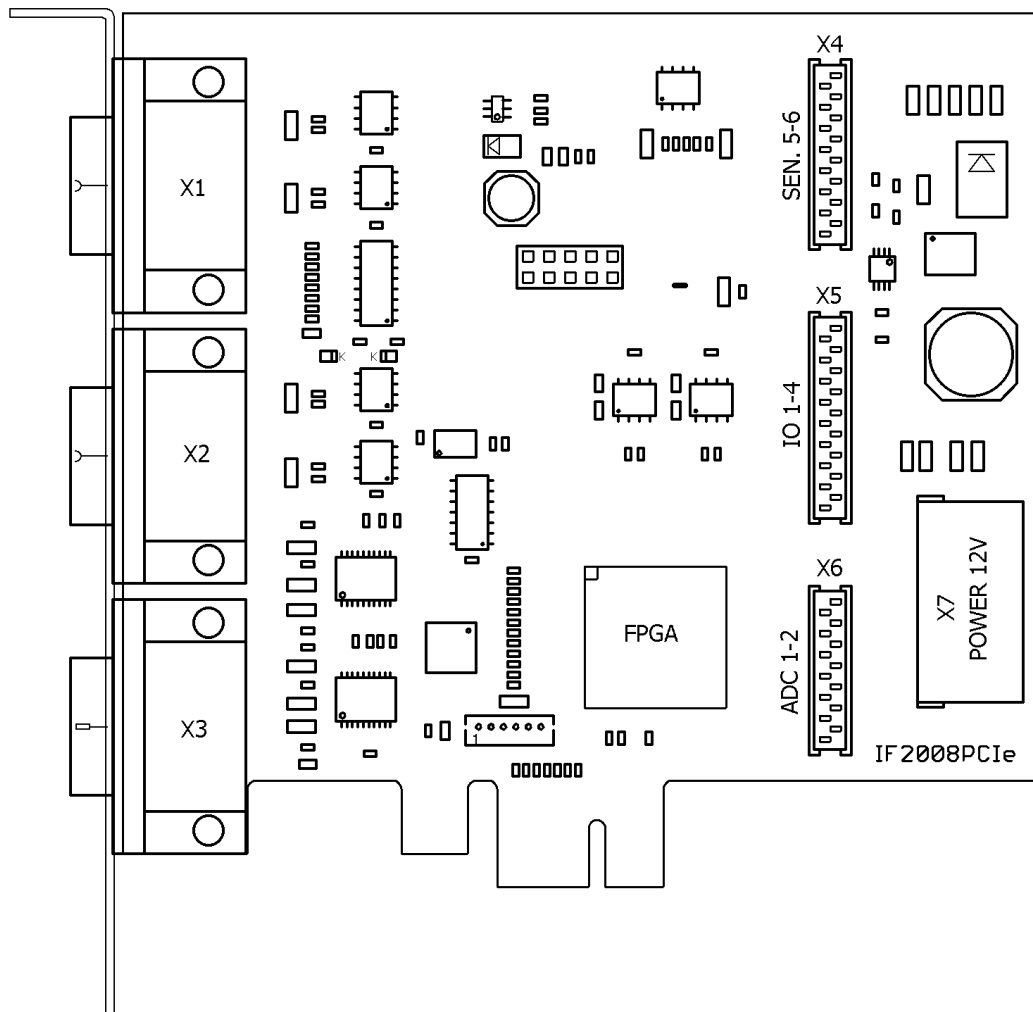


Figure 1: View of board IF2008/PCle Basis Board

- X1 = Sensor connection 1 and 2
- X2 = Sensor connection 3 and 4
- X3 = Encoder connection 1 and 2
- X4 ... X6 = Connector for IF2008E connection
- X7 = Connection 12 V power

## 2.2 View of IF2008E Expansion Board

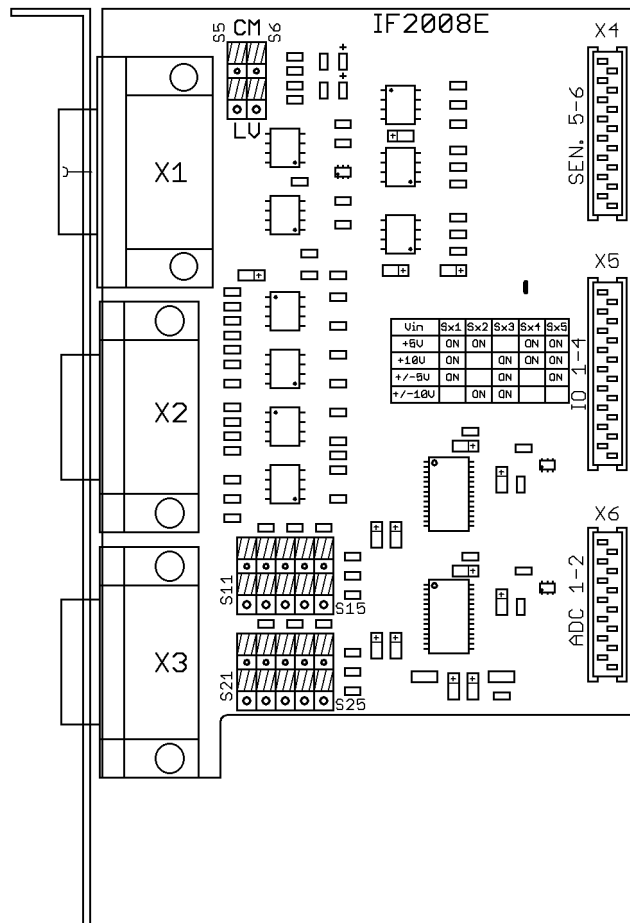


Figure2: View of board IF2008E expansion board

- X1 = Sensor connection 5 and 6
- X2 = Connection for IO signals
- X3 = Connection for A/D converter
- X4 ... X6 = Connection for IF2008/PCle connection
- S5 and S6 = Switch for positive trigger level
- S11 ... S15 = Switch for ADC level 1
- S21 ... S25 = Switch for ADC level 2

### 3 Pin Assignment and Jumper Settings

#### 3.1 Sensor Interface (IF2008/PCIe X1 and X2, IF2008E X1)

Pin	Signal
1	Sensor 1 TxD-
2	Sensor 1 TxD+
3	Sensor 1 RxD-
4	Sensor 1 RxD+
5	GND
6	Sensor 1 TRG+
7	Sensor 1 TRG-
8	Sensor 2 TRG+
9	Sensor 2 TRG-
10	Power supply +24V
11	Sensor 2 TxD-
12	Sensor 2 TxD+
13	Sensor 2 RxD-
14	Sensor 2 RxD+
15	GND

Table 1: Pin assignment for sensor interface

#### 3.2 Encoder Interface (IF2008/PCIe X3)

Pin	Function
1	Encoder 1 Track A+
2	Encoder 1 Track A-
3	Encoder 2 Track A+
4	Encoder 2 Track A-
5	VCC (+5 V)
6	Encoder 1 Track B+
7	Encoder 1 Track B-
8	Encoder 2 Track B+
9	Encoder 2 Track B-
10	GND
11	Encoder 1 Track R+
12	Encoder 1 Track R-
13	Encoder 2 Track R+
14	Encoder 2 Track R-
15	GND

Table 2: Pin assignment for encoder interface

**Attention:** The pin assignment is **not** compatible with IF2004B!

### 3.3 Sensor Power (IF2008/PCIe X7)

Pin	Function
1	+12V
2	GND
3	GND
4	n.c.

Table 3: Pin assignment of sensor power

### 3.4 IO Interface (IF2008E X2)

Pin	Function
1	OUT1
2	OUT2
3	OUT3
4	OUT4
5	GND
6	IN1
7	IN2
8	IN3
9	IN4

Table 4: Pin assignment IO interface

### 3.5 Analog Interface (IF2008E X3)

Pin	Function
1	Input signal 1
2	Analog GND
3	Input signal 2
4	Analog GND
5	n.c.
6	n.c.
7	n.c.
8	n.c.
9	n.c.

Table 5: Pin assignment analog interface



### 3.6 Jumper/Switch Setting for Trigger Level

By means of the switches S5 and S6 (IF2008E) the positive trigger level for the sensor channels 5 and 6 (IF2008A) can be selected. The negative output always has LVDS level.

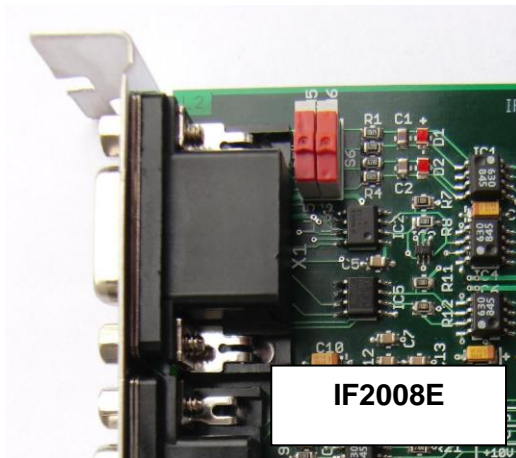


Figure 3: Switch settings trigger level

Switch	Setting	Trigger output +
S5 to S6	LVn	LVDS-Level for sensor n TRG+
	CMn	3.3 V CMOS level for sensor n TRG+

Table 6: Switch settings trigger level

### 3.7 Switch Setting for ADC Level

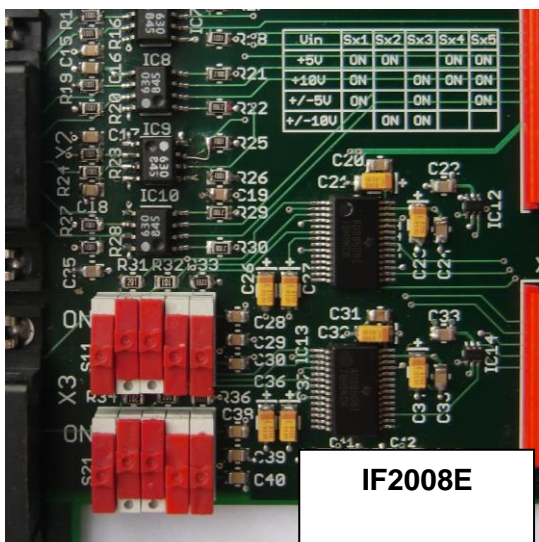


Figure 4: Switch settings ADC level  
( $\pm 10$  V are set in the figure)

VIN	Sx1	Sx2	Sx3	Sx4	Sx5
0-5 V	ON	ON		ON	ON
0-10 V	ON		ON	ON	ON
$\pm 5$ V	ON		ON		ON
$\pm 10$ V		ON	ON		

Table 7: Switch settings ADC level

## 4 Address Assignment

### 4.1 PCI Interface

Interface: PCI-Express x1 interface  
 Access: Memory space 40 Hex addresses  
 Base address: Automatically assigned by operating system

#### Header configuration

Addr.	Byte 3	Byte 2	Byte 1	Byte 0	Value (Hex)
00h	Device ID		Vendor ID		1910 1204
18h	Base Address Local Memory Space				xxxx xxxx
2C	Subsystem ID		Subsystem Vendor ID		2008 1204

Table 8: Header configuration

### 4.2 Local Address Assignment

Base addr. +	Write access	Read access
00h	Transmit register	FIFO data
02h	Set- / Reset- / Latch register	FIFO volume
04h	FIFO enable register	FIFO enable register
06h	Interrupt enable register	Interrupt status register
08h	Sensor 1 baud rate	Reserved
0Ah	Sensor 2 baud rate	Reserved
0Ch	Sensor 3 baud rate	Reserved
0Eh	Sensor 4 baud rate	Reserved
10h	Sensor 5 baud rate	Reserved
12h	Sensor 6 baud rate	Reserved
14h	Counter control register 1	Counter control register 1
16h	Counter control register 2	Counter control register 2
18h	Counter 1 preload LSW	Counter 1 LSW
1Ah	Counter 1 preload MSW	Counter value 1 MSW
1Ch	Counter 2 preload LSW	Counter 2 LSW
1Eh	Counter 2 preload MSW	Counter value 2 MSW
20h	Timer 1 frequency	ADC 1
22h	Timer 1 pulse width	ADC 2
24h	Timer 2 frequency	Status, FPGA-/ hardware version
26h	Timer 2 pulse width	Input and status power switch
28h	Timer 3 frequency	Reserved
2Ah	Timer 3 pulse width	Reserved
2Ch	Timer clock splitter	Timer clock splitter
2Eh	Output register	Output register
30h	Mode opto- and TxD outputs	Mode opto- and TxD outputs
32h	Trigger Outputs Mode	Mode trigger outputs, latch source and sensor power switch
34h	ADC control register	ADC control register
36h	Parity enable register	Parity error

Table 9: Local address assignment

## 5 Register Description

### 5.1 Transmit Register

Base addr. + 00h (write access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			S6	S5	S4	S3	S2	S1	D7	D6	D5	D4	D3	D2	D1	D0
	Selection sensor channel							Data bits								

Table 10: Transmit register

Bits 0 to 7 Include the data for the transmit register

Bits 8 to 15 Select the sensor channel

Bit 8 = 1 → Data are output on the sensor channel S1

Bit 9 = 1 → Data are output on the sensor channel S2

etc.

Bit 13 = 1 → Data are output on the sensor channel S6

Bits 14..15 → free

Immediately on the write access to the address “0”, the data with the bit 8 to 13 selected sensor channel are transmitted. The baud rate for the transmit register is automatically adapted to the selected sensor channel. In case that the data output is effected on more channels, the baud rate of the best channel is used.

### 5.2 FIFO Data

Base addr. + 00h (read access)

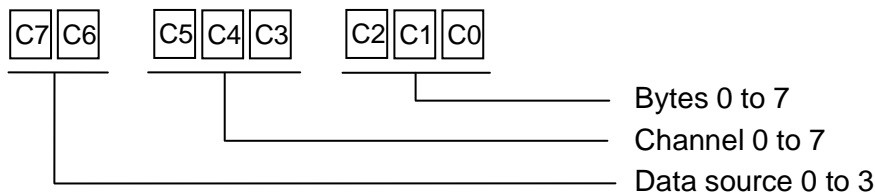
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Code bits							Data bits								

Table 11: FIFO data memory

Bits 0 to 7 Include the data buffered

Bits 8 to 15 Mark the data code

#### Code bits



C7	C6	Data source
0	0	Sensor
0	1	Encoder
1	0	Switching input (IN 1..4 → channel 0, RxD 1..6 → channel 1)
1	1	ADC

Table 12: FIFO data memory – data sources

### 5.3 Set-/ Reset-/ Latch Register

Base addr. + 02h (write access)

Bit	Function
0	Delete counter 1
1	Load counter 1
2	Latch counter 1
3	Reference counter 1
4	Delete counter 2
5	Load counter 2
6	Latch counter 2
7	Reference counter 2
8	Start ADC1 conversion
9	Start ADC2 conversion
10	Delete FIFO
11 – 15	Reserved

Table 13: Set- / Reset- / Latch register

**Please note:**

- By means of the bits 0 to 2 and 4 to 6, the counters can be either deleted or loaded independently of the counter control register by the software, (addr. 14h and addr. 16h). Furthermore, the counter reading can be transferred into the latch register.
- If a counter latch or load function, which should only operate in connection with a reference marker signal is settled by the counter control register (addr. 14h and addr. 16h); this is subject to approval by setting bit 3 or bit 7. On setting bit 3 or bit 7 the status bits 0 and 1 or 2 and 3 are reset.
- All bits only need to be set, resetting them is not necessary.
- After power interruption, all bits are set to "0".

### 5.4 FIFO Volume

Base addr. + 02h (read access)

Bit	Function
0 to 14	FIFO data volume (0 to 32767)
15	permanently 0

Table 14: FIFO volume

The dataset is transferred automatically into the FIFO data memory on receipt. By means of a report of the FIFO volume the FIFO data amount can be calculated. The order and speed regarding buffering the data received, is similar to the data stream of the receiving register. In case that the FIFO is not readout quickly enough, it offers the latest 32768 data sets.

## 5.5 FIFO Enable Register

Base addr. + 04h (read and write access)

Bit	Function
0	0 = FIFO for sensor channel 1 disabled 1 = FIFO for sensor channel 1 enabled
1	0 = FIFO for sensor channel 2 disabled 1 = FIFO for sensor channel 2 enabled
2	0 = FIFO for sensor channel 3 disabled 1 = FIFO for sensor channel 3 enabled
3	0 = FIFO for sensor channel 4 disabled 1 = FIFO for sensor channel 4 enabled
4	0 = FIFO for sensor channel 5 disabled 1 = FIFO for sensor channel 5 enabled
5	0 = FIFO for sensor channel 6 disabled 1 = FIFO for sensor channel 6 enabled
6	0 = FIFO for encoder channel 1 disabled 1 = FIFO for encoder channel 1 enabled
7	0 = FIFO for encoder channel 2 disabled 1 = FIFO for encoder channel 2 enabled
8	0 = FIFO for state of external inputs IN 1..4 disabled 1 = FIFO for state of external inputs IN 1..4 enabled
9	0 = FIFO for state of RxD inputs (sensor 1..6) disabled 1 = FIFO for state of RxD inputs (sensor 1..6) enabled
10	0 = FIFO for ADC 1 disabled 1 = FIFO for ADC 1 enabled
11	0 = FIFO for ADC 2 disabled 1 = FIFO for ADC 2 enabled
12	0 = FIFO is disabled for sensor 1 and 2 if ext. input IN 1 is active 1 = IN 1 does not affect FIFO
13	0 = FIFO is disabled for sensor 3 and 6 if ext. input IN 2 is active 1 = IN 2 does not affect FIFO
14	0 = FIFO is disabled for encoder 1 and 2 if ext. input IN 3 is active 1 = IN 3 does not affect FIFO
15	0 = FIFO is disabled for ADC 1/2; IN 1..4; RxD 1..6 if ext. input IN 4 is active 1 = IN 4 does not affect FIFO

Table 15: FIFO enable register

## 5.6 Interrupt Enable Register

Base addr. + 06h (write access)

Bit	Function
0	1 = Enable interrupt requirements if FIFO is filled with more than 50 %
1	1 = Enable interrupt requirements if FIFO is filled with more than 75 %
2	1 = Enable interrupt requirements on overflow Timer 1
3	1 = Enable interrupt requirements on overflow Timer 2
4	1 = Enable interrupt requirements on overflow Timer 3
5	1 = Enable interrupt requirements if external input IN 1 is activated
6	1 = Enable interrupt requirements if external input IN 2 is activated
7	1 = Enable interrupt requirements if external input IN 3 is activated
8	1 = Enable interrupt requirements if external input IN 4 is activated
9 - 15	Reserved

Table 16: Interrupt enable register

### Please note:

The interrupt generation is controlled by a trigger flange, i.e., an interrupt requirement is only effected if the corresponding bit is set in the interrupt enable register. Furthermore, the appropriate source has to change from the inactive into the active state. Several bits can be set at the same time.

## 5.7 Interrupt Status Register

Base addr. + 06h (read access)

Bit	Function
0	1 = Interrupt requirement if FIFO level exceeds 50%
1	1 = Interrupt requirement if FIFO level exceeds 75%
2	1 = Interrupt requirement on overflow Timer 1
3	1 = Interrupt requirement on overflow Timer 2
4	1 = Interrupt requirement on overflow Timer 3
5	1 = Interrupt requirement if external input IN 1 is activated
6	1 = Interrupt requirement if external input IN 2 is activated
7	1 = Interrupt requirement if external input IN 3 is activated
8	1 = Interrupt requirement if external input IN 4 is activated
9 - 15	Reserved

Table 17: Interrupt status register

### Please note:

The interrupt state register informs by which source(s) the interrupt requirements have been generated. One interrupt requirement can be effected by using more than one source at the same time. In case that no state bit is set, the interrupt requirement was not generated by the IF2008A but by another hardware.

## 5.8 Sensor Baud Rate

Base addr.	Sensor channel	Value	Access
+ 08h	1	1 to 65,535	only write access
+ 0Ah	2	1 to 65,535	only write access
+ 0Ch	3	1 to 65,535	only write access
+ 0Eh	4	1 to 65,535	only write access
+ 10h	5	1 to 65,535	only write access
+ 12h	6	1 to 65,535	only write access

Table 18: Base addresses for sensor baud rates

$$\text{Value} = (48 \text{ MHz} / \text{baud rate}) - 1$$

Example:

Desired baud rate = 691.2 kBaud

Value = (48 MHz / 691,200) - 1 = 68.44

The input value must be a whole number, i.e., the result must still be rounded:

→ **Value = 68**

## 5.9 Counter Control Register

Base addr.	Counter channel	Bit	Access
+ 14h	1	0 to 15	Read and write access
+ 16h	2	0 to 15	Read and write access

Table 19: Base addresses for counter control register

The tables below are the same for both counter channels!

### Overview of Functions

Bit	Function
0 to 3	Interpolation (see Table 21: Encoder interpolation)
4	Counting direction (see Table 22: Encoder counter direction)
5 to 7	Counter mode (see Table 23: Counter mode)
8 to 11	Latch source (see Table 24: Counter latch source)
12 to 15	Reserved

Table 20: Functional overview for counter control register

**Interpolation**

Bit 3	Bit 2	Bit 1	Bit 0	Interpolation
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	10
1	0	0	0	12
1	0	0	1	16
1	0	1	0	20
1	0	1	1	24
1	1	0	0	32
1	1	0	1	40
1	1	1	0	48
1	1	1	1	64

Table 21: Encoder interpolation

**Please note:**

- For encoders with 1-Vss signals all interpolations are suitable
- For encoders with TTL-signals the following interpolations are suitable: 1, 2 or 4 times

**Counting direction**

Bit 4	Counting direction
0	normal
1	inversed

Table 22: Encoder counter direction

**Counter mode:**

Bit 7	Bit 6	Bit 5	Counter mode						
0	0	0	No counter load / delete function by encoder reference marker						
0	0	1	Counter is loaded with the next encoder reference marker provided that the state bit 0 or state bit 2 "0" is settled.						
0	1	0	Counter is loaded including all encoder reference markers and load register content. State bit 0 to 3 have no effect.						
0	1	1	Counter is deleted including all encoder reference markers and additionally loaded with the content of the load register if the counter has reached -1. This function offers the possibility to limit the counter. During this process the counter load register has to be preallocated with the number of increments limited -1.						
1	0	0	Counter without phase discriminator (event counter) <table border="1" data-bbox="628 1733 1430 1928"> <thead> <tr> <th>Bit 4</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Track A = counter direction signal Track B = counter clock signal</td> </tr> <tr> <td>1</td> <td>Track A = counter clock signal Track B = counter direction signal</td> </tr> </tbody> </table>	Bit 4	Function	0	Track A = counter direction signal Track B = counter clock signal	1	Track A = counter clock signal Track B = counter direction signal
Bit 4	Function								
0	Track A = counter direction signal Track B = counter clock signal								
1	Track A = counter clock signal Track B = counter direction signal								
1	0	1	Reserved						
1	1	0	Reserved						
1	1	1	Reserved						

Table 23: Counter mode



**Latch source:**

Bit 11	Bit 10	Bit 9	Bit 8	Latch source
0	0	0	0	Hardware latch disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E expansion board)
1	0	1	1	IN 2 (only with IF2008E expansion board)
1	1	0	0	IN 3 (only with IF2008E expansion board)
1	1	0	1	IN 4 (only with IF2008E expansion board)
1	1	1	0	2nd reference mark
1	1	1	1	all reference marks

Table 24: Counter latch source

**5.10 Counter Preload**

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65,535	only write access
+ 1Ah	1 MSW	0 to 65,535	only write access
+ 1Ch	2 LSW	0 to 65,535	only write access
+ 1Eh	2 MSW	0 to 65,535	only write access

Table 25: Base addresses for counter preload

**5.11 Counter Value**

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65,535	only read access
+ 1Ah	1 MSW	0 to 65,535	only read access
+ 1Ch	2 LSW	0 to 65,535	only read access
+ 1Eh	2 MSW	0 to 65,535	only read access

Table 26: Base addresses for counter value

## 5.12 Timer

Base addr.	Timer	Value	Access
+ 20h	1 frequency	0 to 65,535	only write access
+ 22h	1 pulse width	0 to 65,535	only write access
+ 24h	2 frequency	0 to 65,535	only write access
+ 26h	2 pulse width	0 to 65,535	only write access
+ 28h	3 frequency	0 to 65,535	only write access
+ 2Ah	3 pulse width	0 to 65,535	only write access
+ 2Ch	Clock splitter		Read and write access

Table 27: Base addresses for timer

$$\text{Value}(F) = (F_{\text{Clock}} / F_{\text{OUT}}) - 1$$

$$\text{Value}(PW) = (PW_{\text{OUT}} / T_{\text{Clock}})$$

### Example:

Desired frequency  $F_{\text{OUT}} = 10 \text{ kHz}$

Desired pulse width  $PW_{\text{OUT}} = 25 \mu\text{s}$

Clock splitter = 0  $\rightarrow F_{\text{Clock}} = 24 \text{ MHz}$ ,  $T_{\text{Clock}} = 41.667 \text{ ns}$  (see the following table for clock splitter)

$$\text{Value}(F) = (24 \text{ MHz} / 10 \text{ kHz}) - 1 = 2399$$

$$\text{Value}(PW) = (25 \mu\text{s} / 41.667 \text{ ns}) = 600$$

The input values must be whole numbers!

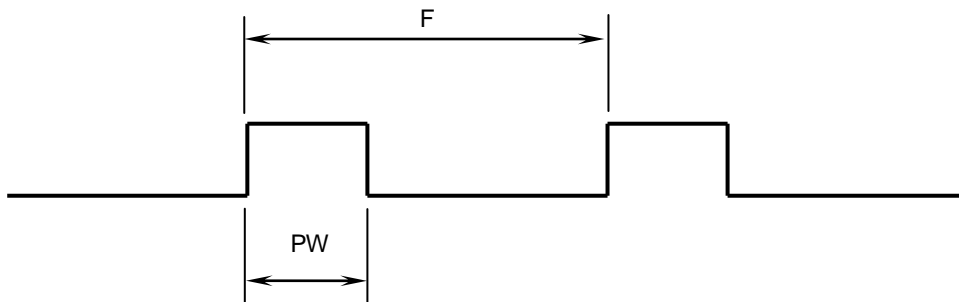


Figure 5: Timer frequency and pulse width

### Please note:

The pulse width only affects the “sensor trigger” and “optocoupler” outputs and not the internal synchronization signals. For this, the zero crossing timer is used.

To turn off the timer, the frequency must be programmed to be "0". If pulse width > 0 is programmed when the timer is turned off, output is permanently set to High. However, if the pulse width is also programmed to be "0", output is permanently set to Low.

**Clock Splitter:**

Bit 3	Bit 2	Bit 1	Bit 0	Clock frequency timer 1
Bit 7	Bit 6	Bit 5	Bit 4	Clock frequency timer 2
Bit 11	Bit 10	Bit 9	Bit 8	Clock frequency timer 3
0	0	0	0	24 MHz
0	0	0	1	24 MHz / 2
0	0	1	0	24 MHz / 4
0	0	1	1	24 MHz / 8
0	1	0	0	24 MHz / 16
0	1	0	1	24 MHz / 32
0	1	1	0	24 MHz / 64
0	1	1	1	24 MHz / 128
1	0	0	0	24 MHz / 256
1	0	0	1	24 MHz / 512
1	0	1	0	24 MHz / 1024
1	0	1	1	24 MHz / 2048
1	1	0	0	24 MHz / 4096
1	1	0	1	24 MHz / 8192
1	1	1	0	24 MHz / 16384
1	1	1	1	24 MHz / 32768

Table 28: Timer clock splitter

**Please note:**

Bit 12 to Bit 15 are reserved.

**5.13 ADC**

Base addr.	ADC channel	Value	Access
+ 20h	1	0 to 65535	only read access
+ 22h	2	0 to 65535	only read access

Table 29: Base addresses for ADC

## 5.14 State

Base addr. + 24h (only read access)

Bit	Function
0	1 = Encoder 1: 1st reference mark crossed
1	1 = Encoder 1: 2nd reference mark crossed
2	1 = Encoder 2: 1st reference mark crossed
3	1 = Encoder 2: 2nd reference mark crossed
4	0 = Transmitter ready for new data transfer 1 = Transmitter is occupied
5	0 = No extension module with sensor 5 / 6 available 1 = Extension module with sensor 5 / 6 available
6	0 = No extension module for external I/O available 1 = Extension module for external I/O available
7	0 = No extension module with ADC available 1 = Extension module with ADC available
8 – 13	FPGA version
14 – 15	Hardware version

Table 30: Status

## 5.15 Input and Sensor Power Switch Status

Base addr. + 26h (only read access)

Bit	Function
0	1 = Ext. input IN 1 active
1	1 = Ext. input IN 2 active
2	1 = Ext. input IN 3 active
3	1 = Ext. input IN 4 active
4	1 = RxD input on the sensor input 1 active
5	1 = RxD input on the sensor input 2 active
6	1 = RxD input on the sensor input 3 active
7	1 = RxD input on the sensor input 4 active
8	1 = RxD input on the sensor input 5 active
9	1 = RxD input on the sensor input 6 active
10	1 = Error sensor power switch
11 – 15	Reserved

Table 31: Input und sensor power switch

## 5.16 Output Register

Base addr. + 2Eh (read and write access)

Bit	Function	Output signal
0	0 = OUT 1 OFF    Optocoupler disabled 1 = OUT 1 ON    Optocoupler conductive	Output 1 = High Output 1 = Low
1	0 = OUT 2 OFF    Optocoupler disabled 1 = OUT 2 ON    Optocoupler conductive	Output 2 = High Output 2 = Low
2	0 = OUT 3 OFF    Optocoupler disabled 1 = OUT 3 ON    Optocoupler conductive	Output 3 = High Output 3 = Low
3	0 = OUT 4 OFF    Optocoupler disabled 1 = OUT 4 ON    Optocoupler conductive	Output 4 = High Output 4 = Low
4	0 = TxD 1    inactive 1 = TxD 1    active	TxD 1+ = High    TxD 1- = Low TxD 1+ = Low    TxD 1- = High
5	0 = TxD 2    inactive 1 = TxD 2    active	TxD 2+ = High    TxD 2- = Low TxD 2+ = Low    TxD 2- = High
6	0 = TxD 3    inactive 1 = TxD 3    active	TxD 3+ = High    TxD 3- = Low TxD 3+ = Low    TxD 3- = High
7	0 = TxD 4    inactive 1 = TxD 4    active	TxD 4+ = High    TxD 4- = Low TxD 4+ = Low    TxD 4- = High
8	0 = TxD 5    inactive 1 = TxD 5    active	TxD 5+ = High    TxD 5- = Low TxD 5+ = Low    TxD 5- = High
9	0 = TxD 6    inactive 1 = TxD 6    active	TxD 6+ = High    TxD 6- = Low TxD 6+ = Low    TxD 6- = High
10	0 = TRG 1    inactive 1 = TRG 1    active	TRG 1+ = Low    TRG 1- = High TRG 1+ = High    TRG 1- = Low
11	0 = TRG 2    inactive 1 = TRG 2    active	TRG 2+ = Low    TRG 2- = High TRG 2+ = High    TRG 2- = Low
12	0 = TRG 3    inactive 1 = TRG 3    active	TRG 3+ = Low    TRG 3- = High TRG 3+ = High    TRG 3- = Low
13	0 = TRG 4    inactive 1 = TRG 4    active	TRG 4+ = Low    TRG 4- = High TRG 4+ = High    TRG 4- = Low
14	0 = TRG 5    inactive 1 = TRG 5    active	TRG 5+ = Low    TRG 5- = High TRG 5+ = High    TRG 5- = Low
15	0 = TRG 6    inactive 1 = TRG 6    active	TRG 6+ = Low    TRG 6- = High TRG 6+ = High    TRG 6- = Low

Table 32: Output register

### Please note:

For all outputs, several signal sources are available. Bits listed above are only connected through in case that the appropriate mode is set (see Table 33: Mode Opto- and TxD Outputs on page 22).

<sup>1)</sup> Possible only with expansion board

## 5.17 Mode Opto- and TxD Outputs

Base addr. + 30h (read and write access)

Bit	Function		
0 and 1	<b>Bit 1</b>	<b>Bit 0</b>	<b>Function</b>
	0	0	Output 1 switches Bit 0 with addr. 2Eh
	0	1	Output 1 switches pulse width with Timer 1
	1	0	Output 1 switches pulse width with Timer 2
	1	1	Output 1 switches pulse width with Timer 3
2 and 3	<b>Bit 3</b>	<b>Bit 2</b>	<b>Function</b>
	0	0	Output 2 switches Bit 1 with addr. 2Eh
	0	1	Output 2 switches pulse width with Timer 1
	1	0	Output 2 switches pulse width with Timer 2
	1	1	Output 2 switches pulse width with Timer 3
4 and 5	<b>Bit 5</b>	<b>Bit 4</b>	<b>Function</b>
	0	0	Output 3 switches Bit 2 with addr. 2Eh
	0	1	Output 3 switches pulse width with Timer 1
	1	0	Output 3 switches pulse width with Timer 2
	1	1	Output 3 switches pulse width with Timer 3
6 and 7	<b>Bit 7</b>	<b>Bit 6</b>	<b>Function</b>
	0	0	Output 4 switches Bit 3 with addr. 2Eh
	0	1	Output 4 switches pulse width with Timer 1
	1	0	Output 4 switches pulse width with Timer 2
	1	1	Output 4 switches pulse width with Timer 3
8	0 = TxD 1 switches with transmitter 1 = TxD 1 switches bit 4 with addr. 2Eh		
9	0 = TxD 2 switches with transmitter 1 = TxD 2 switches bit 5 with addr. 2Eh		
10	0 = TxD 3 switches with transmitter 1 = TxD 3 switches bit 6 with addr. 2Eh		
11	0 = TxD 4 switches with transmitter 1 = TxD 4 switches bit 7 with addr. 2Eh		
12	0 = TxD 5 switches with transmitter 1 = TxD 5 switches bit 8 with addr. 2Eh		
13	0 = TxD 6 switches with transmitter 1 = TxD 6 switches bit 9 with addr. 2Eh		
14 - 15	Reserved		

Table 33: Mode Opto- and TxD Outputs

**Please note:**

The outputs 1 to 4 are only available for the IF2008E expansion board.

## 5.18 Mode Trigger Outputs, Latch Source and Sensor Power Switch

Base addr. + 32h (read and write access)

Bit	Function		
0 and 1	<b>Bit 1</b>	<b>Bit 0</b>	<b>Function</b>
	0	0	Trigger 1 switches Bit 10 with addr. 2Eh
	0	1	Trigger 1 switches pulse width with Timer 1
	1	0	Trigger 1 switches pulse width with Timer 2
	1	1	Trigger 1 switches pulse width with Timer 3
2 and 3	<b>Bit 3</b>	<b>Bit 2</b>	<b>Function</b>
	0	0	Trigger 2 switches Bit 11 with addr. 2Eh
	0	1	Trigger 2 switches pulse width with Timer 1
	1	0	Trigger 2 switches pulse width with Timer 2
	1	1	Trigger 2 switches pulse width with Timer 3
4 and 5	<b>Bit 5</b>	<b>Bit 4</b>	<b>Function</b>
	0	0	Trigger 3 switches Bit 12 with addr. 2Eh
	0	1	Trigger 3 switches pulse width with Timer 1
	1	0	Trigger 3 switches pulse width with Timer 2
	1	1	Trigger 3 switches pulse width with Timer 3
6 and 7	<b>Bit 7</b>	<b>Bit 6</b>	<b>Function</b>
	0	0	Trigger 4 switches Bit 13 with addr. 2Eh
	0	1	Trigger 4 switches pulse width with Timer 1
	1	0	Trigger 4 switches pulse width with Timer 2
	1	1	Trigger 4 switches pulse width with Timer 3
8 and 9	<b>Bit 9</b>	<b>Bit 8</b>	<b>Function</b>
	0	0	Trigger 5 switches Bit 14 with addr. 2Eh
	0	1	Trigger 5 switches pulse width with Timer 1
	1	0	Trigger 5 switches pulse width with Timer 2
	1	1	Trigger 5 switches pulse width with Timer 3
10 and 11	<b>Bit 11</b>	<b>Bit 10</b>	<b>Function</b>
	0	0	Trigger 6 switches Bit 15 with addr. 2Eh
	0	1	Trigger 6 switches pulse width with Timer 1
	1	0	Trigger 6 switches pulse width with Timer 2
	1	1	Trigger 6 switches pulse width with Timer 3

Bit	Function			
12 – 14	<b>Bit 14</b>	<b>Bit 13</b>	<b>Bit 12</b>	<b>Latch source</b>
	0	0	0	Hardware latch disabled
	0	0	1	Timer 1
	0	1	0	Timer 2
	0	1	1	Timer 3
	1	0	0	Sensor channel 1
	1	0	1	Sensor channel 2
	1	1	0	Sensor channel 3
1	1	1	Sensor channel 4	
15	Bit 15 = 0      Sensor power ON (default value after Reset)			
	Bit 15 = 1      Sensor power OFF			

Table 34: Mode trigger outputs, latch source and sensor power switch

**Please note:**

Bits 12 to 14 can be used to select a latch source whose trigger event writes the external trigger inputs (IN 1 to 4) and the RxD inputs (sensor 1 to 6) to FIFO.



## 5.19 ADC Control Register

Base addr. + 34h (read and write access)

Bit 3	Bit 2	Bit 1	Bit 0	Conversion source ADC1
Bit 7	Bit 6	Bit 5	Bit 4	Conversion source ADC2
0	0	0	0	Hardware conversion disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E expansion board)
1	0	1	1	IN 2 (only with IF2008E expansion board)
1	1	0	0	IN 3 (only with IF2008E expansion board)
1	1	0	1	IN 4 (only with IF2008E expansion board)
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 35: ADC control register bits 0-7

Bit	Function
8	0 = ADC1 data output binary 2-complement 1 = ADC1 data output binary unconverted
9	0 = ADC2 data output binary 2-complement 1 = ADC2 data output binary unconverted
10 – 15	Reserved

Table 36: ADC control register bits 8-15

Analog input				Digital output	
0 – 5 V	0 – 10 V	+/-5 V	+/-10 V	Binary 2-complement	Binary unconverted
+4.99V	+9.99V	+4.99V	+9.99V	7FFF	FFFF
2.5V	5V	0V	0V	0000	8000
+2.499V	+4.999V	-153 $\mu$ V	-305 $\mu$ V	FFFF	7FFF
0V	0V	-5V	-10V	8000	0000

Table 37: ADC converting result

## 5.20 Parity Enable Register

Base addr. + 36h (write access)

Bit	Function
0	0 = Parity bit for sensor channel 1 disabled 1 = Parity bit for sensor channel 1 enabled (only even parity)
1	0 = Parity bit for sensor channel 2 disabled 1 = Parity bit for sensor channel 2 enabled (only even parity)
2	0 = Parity bit for sensor channel 3 disabled 1 = Parity bit for sensor channel 3 enabled (only even parity)
3	0 = Parity bit for sensor channel 4 disabled 1 = Parity bit for sensor channel 4 enabled (only even parity)
4	0 = Parity bit for sensor channel 5 disabled 1 = Parity bit for sensor channel 5 enabled (only even parity)
5	0 = Parity bit for sensor channel 6 disabled 1 = Parity bit for sensor channel 6 enabled (only even parity)
6-15	Reserved

Table 38: Parity enable register

## 5.21 Parity Error Register

Base addr. + 36h (read access)

Bit	Function
0	1 = Parity-Error sensor channel 1
1	1 = Parity-Error sensor channel 2
2	1 = Parity-Error sensor channel 3
3	1 = Parity-Error sensor channel 4
4	1 = Parity-Error sensor channel 5
5	1 = Parity-Error sensor channel 6
6 – 15	Reserved

Table 39: Parity error register

## 6 Wiring Recommendations

### 6.1 Sensor ILD1420

Pin IF2008/PCle	Signal IF2008/PCle	ILD1420		Signal ILD1420
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	4		RxD-
2	Sensor 1 TxD+	3		RxD+
3	Sensor 1 RxD-	6		TxD-
4	Sensor 1 RxD+	5		TxD+
5	Power supply 0V	12	12	GND
6	Sensor 1 TRG+	9		TeachIn
7	Sensor 1 TRG-	n.c.	n.c.	
8	Sensor 2 TRG+		9	TeachIn
9	Sensor 2 TRG-	n.c.	n.c.	
10	Power supply +24V	7	7	+UB
11	Sensor 2 TxD-		4	RxD-
12	Sensor 2 TxD+		3	RxD+
13	Sensor 2 RxD-		6	TxD-
14	Sensor 2 RxD+		5	TxD+
15	GND (galvanically separated to GND PC)	12	12	GND

Table 40: Sensor wiring ILD1420

### 6.2 Sensor ILD1750

Pin IF2008/PCle	Signal IF2008/PCle	ILD1750		Signal ILD1750
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	11		RxD-
2	Sensor 1 TxD+	12		RxD+
3	Sensor 1 RxD-	2		TxD-
4	Sensor 1 RxD+	1		TxD+
5	Power supply 0V	6	6	GND
6	Sensor 1 TRG+	3		TRG+
7	Sensor 1 TRG-	4		TRG-
8	Sensor 2 TRG+		3	TRG+
9	Sensor 2 TRG-		4	TRG-
10	Power supply +24V	5	5	+UB
11	Sensor 2 TxD-		11	RxD-
12	Sensor 2 TxD+		12	RxD+
13	Sensor 2 RxD-		2	TxD-
14	Sensor 2 RxD+		1	TxD+
15	GND (galvanically separated to GND PC)	6	6	GND

Table 41: Sensor wiring ILD1750

### 6.3 Sensor ILD2300

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD2300		Signal ILD2300
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	8		RxD-
2	Sensor 1 TxD+	7		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	9		TxD+
5	Power supply 0V	2	2	Supply ground
6	Sensor 1 TRG+	5		SyncIn+
7	Sensor 1 TRG-	6		
8	Sensor 2 TRG+		5	SyncIn+
9	Sensor 2 TRG-		6	
10	Power supply +24V	1	1	+UB
11	Sensor 2 TxD-		8	RxD-
12	Sensor 2 TxD+		7	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		9	TxD+
15	GND (galvanically separated to GND PC)	2	2	SyncIn-

Table 42: Sensor wiring ILD2300

## 6.4 Encoder Interface

Pin IF2008/PCIE	Signal IF2008/PCIE	1Vss or RS422		TTL (single-ended)	
		Signal Encoder 1	Signal Encoder 2	Signal Encoder 1	Signal Encoder 2
1	Encoder 1 Track A+	A+		A	
2	Encoder 1 Track A-	A-		open	
3	Encoder 2 Track A+		A+		A
4	Encoder 2 Track A-		A-		open
5	VCC (+5 V)	+UB	+UB	+UB	+UB
6	Encoder 1 Track B+	B+		B	
7	Encoder 1 Track B-	B-		open	
8	Encoder 2 Track B+		B+		B
9	Encoder 2 Track B-		B-		open
10	GND	GND	GND	GND	GND
11	Encoder 1 Track R+	R+		R	
12	Encoder 1 Track R-	R-		open	
13	Encoder 2 Track R+		R+		R
14	Encoder 2 Track R-		R-		open
15	GND	GND	GND	GND	GND

Table 43: Encoder interface

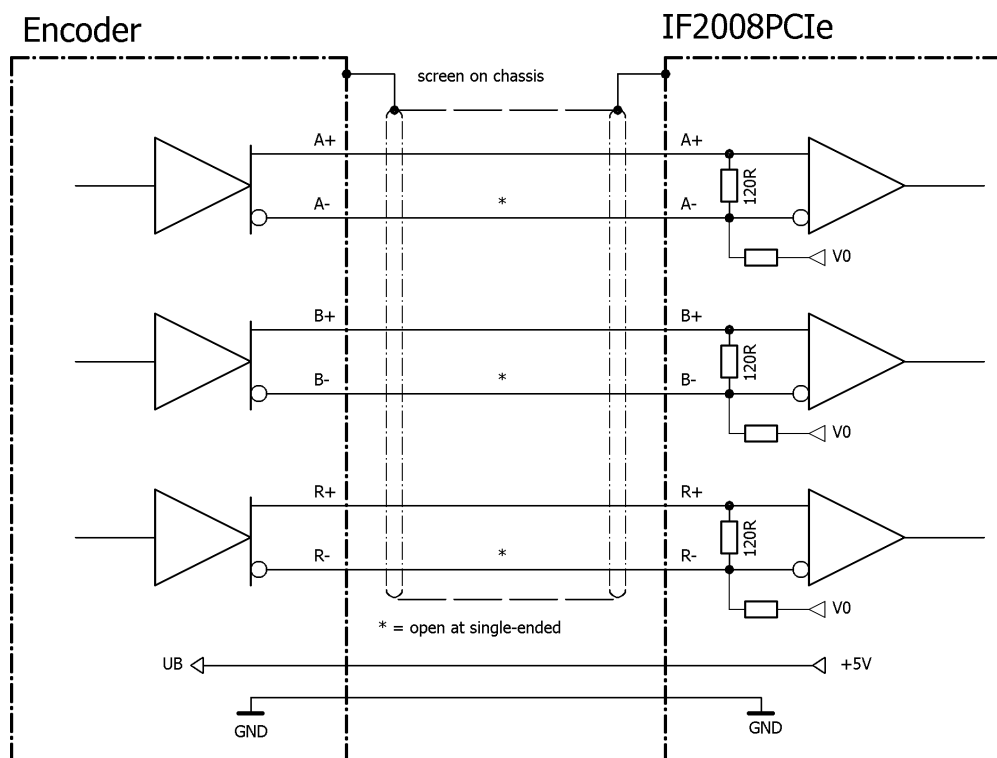


Figure 6: Block diagram encoder interface

**Please note:**

Plus inputs (A+, B+, R+) may not remain open. For example, if only the clock signal is used, the plus inputs have to be set on GND or VCC.

### 6.5 Optocoupler I/O

Pin IF2008/PCIe	Signal IF2008/PCIe
1	OUT1
2	OUT2
3	OUT3
4	OUT4
5	GND
6	IN1
7	IN2
8	IN3
9	IN4

Table 44: Optocoupler I/O

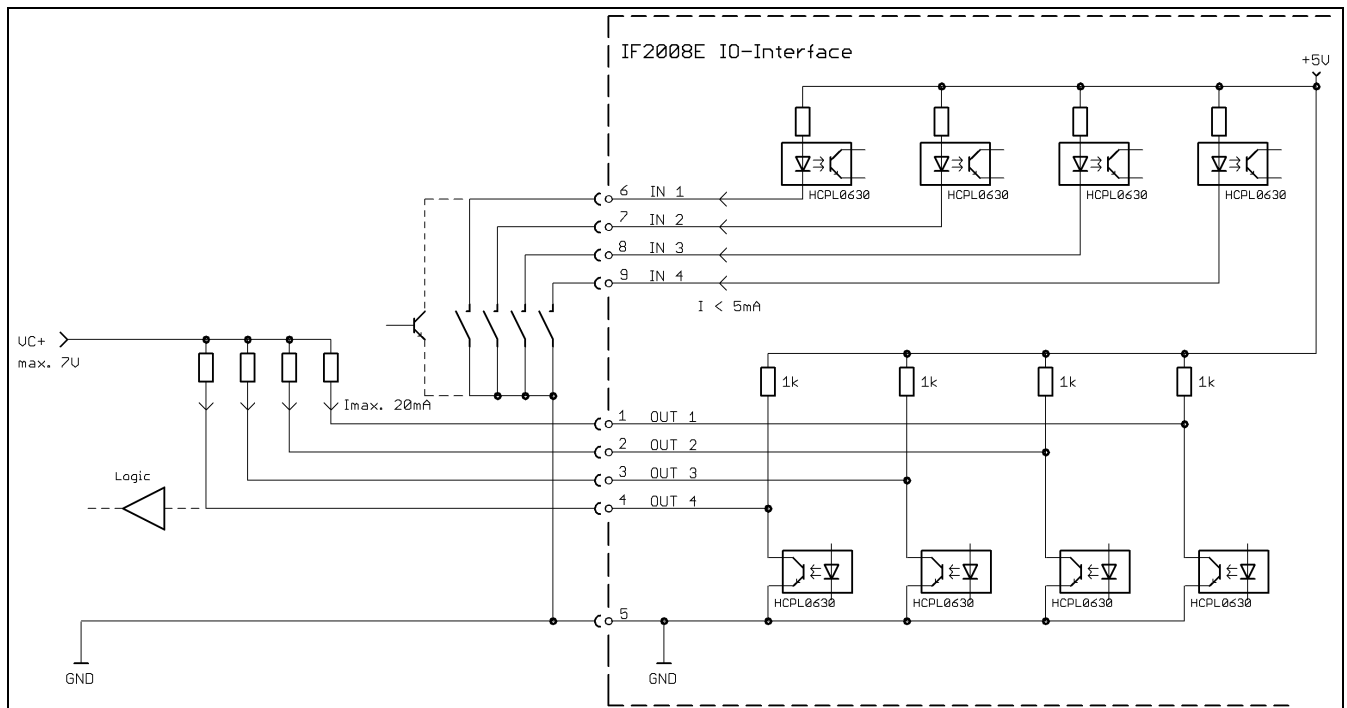


Figure 7: Block diagram optocoupler I/O

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